Logic Synthesis and Verification Algorithms

Gary D. Hachtel, Fabio Somenzi

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Logic Synthesis and Verification Algorithms is a textbook designed for courses on VLSI Logic Synthesis and Verification, Design Automation, CAD and advanced level discrete mathematics. It also serves as a basic reference work in design automation for both professionals and students.

Logic Synthesis and Verification Algorithms is about the theoretical underpinnings of VLSI (Very Large Scale Integrated Circuits). It combines and integrates modern developments in logic synthesis and formal verification with the more traditional matter of Switching and Finite Automata Theory. The book also provides background material on Boolean algebra and discrete mathematics.

A unique feature of this text is the large collection of solved problems.

Throughout the text the algorithms covered are the subject of one or more problems based on the use of available synthesis programs.

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